Amendments to the Claims:

Please amend the claims to read as provided in the following claim listing.

1.-64. (Canceled).

65. (Previously presented) An integrated circuit fabricated on a chip, comprising:

multiple on-chip logic analyzers each including a trigger word recognizer; and

an on-chip memory that captures data in response to match signals from the trigger word recognizers.

66. (Previously presented) The integrated circuit of claim 65, wherein the match signals are each available as a condition to at least one other on-chip logic analyzer.

67. (Previously presented) The integrated circuit of claim 65, wherein the match signals are each available for capture by the on-chip memory.

68. (Previously presented) The integrated circuit of claim 65, wherein the match signals are each provided as an output of the chip.

69. (Previously presented) The integrated circuit of claim 65, wherein each of the multiple on-chip logic analyzers further includes a storage word recognizer.

70. (Previously presented) The integrated circuit of claim 69, wherein the storage word recognizers control per-sample storage of data in an on-chip memory.

71. (Previously presented) The integrated circuit of claim 65, wherein the trigger word recognizers each comprise a Boolean logic section and a

counter/timer section, wherein the Boolean logic section includes multiple hardware match logical units that compare a match value with internal state data and produce an output signal that is true if the comparison indicates a match condition, and wherein each output signal of a hardware match logical units connects to both an AND term and an OR term, and a user selects whether the AND term or the OR term is enabled for each of the hardware match logical units.

72. (Previously presented) The integrated circuit of claim 71, wherein for each trigger word recognizer, the hardware match logical units for which the AND term is selected have their output signals combined together in an AND gate, and all the hardware match logical units for which the OR term is selected have their output signals combined together in an OR gate.

73. (Previously presented) The integrated circuit of claim 72, wherein the output of the AND gate and the output of the OR gate are selectively combined together in one of either an AND operation, an OR operation, a NAND operation, or a NOR operation, wherein the selective combining is performed via a multiplexer.

74. (Previously presented) The integrated circuit of claim 73, wherein the multiplexer output is selectively coupled to a second multiplexer via two different signal paths, and wherein the first signal path remains asserted if a match condition exists, and the second signal path is asserted for a first clock that the match condition exists, and wherein the second multiplexer selects one of the first or second signal path based on a select bit that is programmed by the user.

75. (Previously presented) The integrated circuit of claim 71, wherein the Boolean logic section includes multiple software match logical units that each receive a software-provided match value and produce an output signal that is true if the software-provided match value is true, and wherein each output signal of the software match logical units connects to both an AND term and an OR term,

and the user selects whether the AND term or the OR term is enabled for each of the software match logical units.

76. (Previously presented) The integrated circuit of claim 75, wherein each software match logical unit receives a software-provided match value indicative of one or more non-hardware states in a set consisting of a thread ID, an address-based number, and an interrupt-enable level.

77. (Canceled).

78. (Currently amended) ~~The integrated circuit of claim 77,~~ An integrated circuit fabricated on a chip, comprising:

an on-chip logic analyzer that comprises a trigger word recognizer and a storage word recognizer; and

an on-chip memory that captures data determined by the storage word recognizer in response to a match signal from the trigger word recognizer,

wherein the on-chip logic analyzer is one of multiple on-chip logic analyzers each comprising a trigger word recognizer and a storage word recognizer, and

wherein the on-chip logic analyzer is one of multiple on-chip logic analyzers each comprising a trigger word recognizer and a storage word recognizer.

79. (Previously presented) The integrated circuit of claim 78, wherein the word recognizers each provide a match signal that is available as a condition to at least one corresponding word recognizer in another on-chip logic analyzer.

80. (Currently amended) ~~The integrated circuit of claim 77,~~ An integrated circuit fabricated on a chip, comprising:

an on-chip logic analyzer that comprises a trigger word recognizer and a storage word recognizer; and

an on-chip memory that captures data determined by the storage word recognizer in response to a match signal from the trigger word recognizer,

wherein the word recognizers each comprise a Boolean logic section and a counter/timer section, wherein the Boolean logic section includes multiple hardware match logical units that compare a match value with internal state data and produce an output signal that is true if the comparison indicates a match condition, and wherein each said output signal of the hardware match logical units connects to both an AND term and an OR term, and a user selects whether the AND term or the OR term is enabled for each of the hardware match logical units.

81. (Previously presented) The integrated circuit of claim 80, wherein for each word recognizer, the hardware match logical units for which the AND term is selected have their output signals combined together in an AND gate, and all the hardware match logical units for which the OR term is selected have their output signals combined together in an OR gate.

82. (Previously presented) The integrated circuit of claim 81, wherein the output of the AND gate and the output of the OR gate are selectively combined together in one of either an AND operation, an OR operation, a NAND operation, or a NOR operation, wherein the selective combining is performed via a multiplexer.

83. (Previously presented) The integrated circuit of claim 82, wherein the multiplexer output is selectively coupled to a second multiplexer via two different signal paths, and wherein the first signal path remains asserted if a match condition exists, and the second signal path is asserted for the first clock period

that the match condition exists, and wherein the second multiplexer selects one of the first or second signal path based on a select bit that is programmed by the user.

84. (Previously presented) The integrated circuit of claim 80, wherein the Boolean logic section includes multiple software match logical units that receive a software-provided match value and produce an output signal that is true if the software-provided match value is true, and wherein each said output signal of the software match logical units connects to both an AND term and an OR term, and the user selects whether the AND term or the OR term is enabled for each of the software match logical units.

85. (Previously presented) The integrated circuit of claim 84, wherein each software-provided match value is indicative of one or more non-hardware states in a set consisting of a thread ID, an address-based number, and an interrupt level.